

# Dividing Transactional Memories by Zero

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Transact 2008

# A TM Story

TM implementations

# A TM Story

TM implementations

evaluated with

skip lists, hash tables, ...

# A TM Story

## STMBench7

a benchmark for all TMs

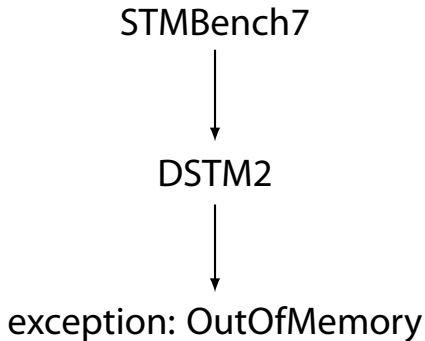
# A TM Story

STMBench7



DSTM2

# A TM Story



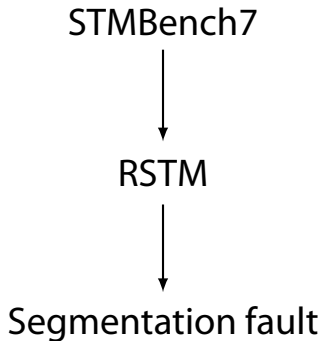
# A TM Story

STMBench7

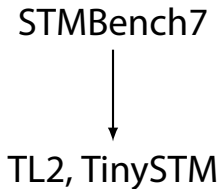


RSTM

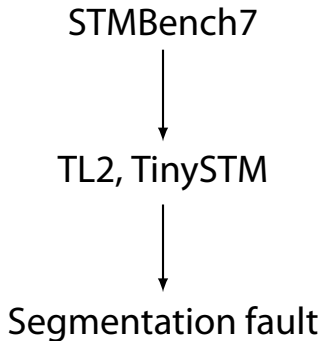
# A TM Story



# A TM Story



# A TM Story



?

# The Goal of STMBench7

Test  
performance  
and usability

# My Goal Today

Show that STMBench7 is a

**valuable tool**

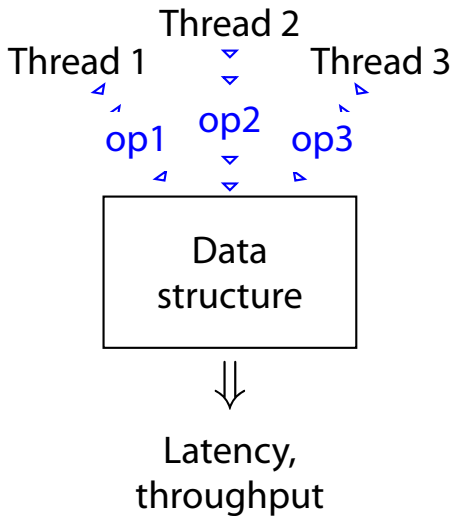
for measuring performance & usability of TMs

# Outline

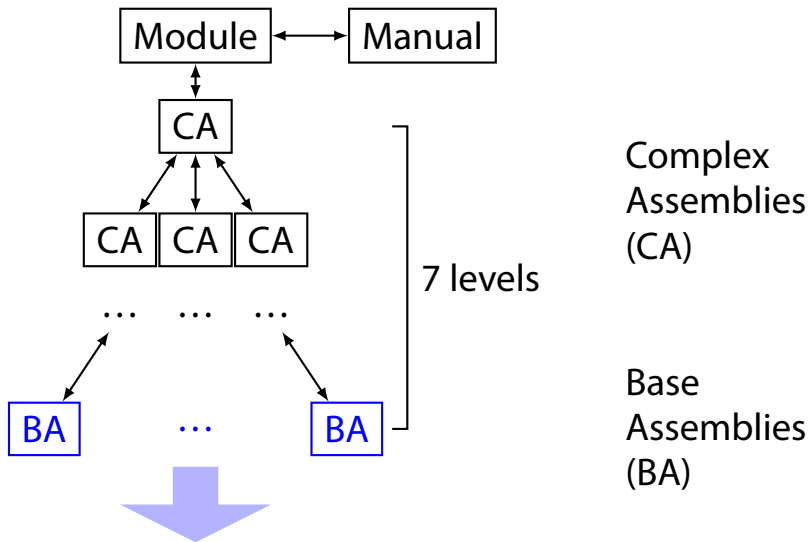
- 1 STMBench7
- 2 Performance results examples

# The STMBench7 Benchmark for TMs

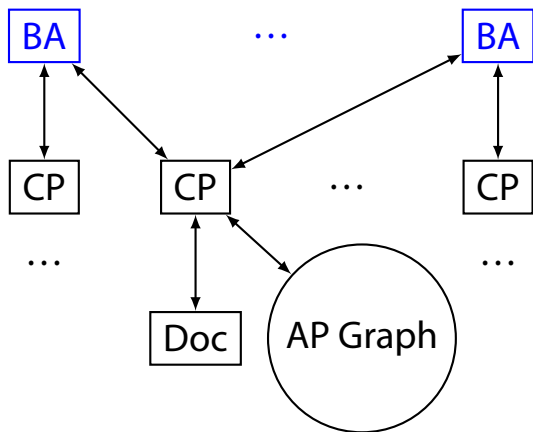
- Real-world workload (CAD/CAM/...)
- Large, complex & dynamic structure
- Various-length operations



# STMBench7 Main Tree



# STMBench7 Design Library



Base Assemblies  
(BA)

Composite Parts  
(CP)

Atomic Parts (AP)

+ indexes

# STMBench7 Features

- Large data structure  
unforgiving for large per-object overheads
- Short and long operations  
“explode” non-linear algorithms
- Complex access patterns  
test policies, not only raw performance
- Complex objects, inheritance  
OO features check
- Use of standard libraries  
usability test

# Outline

1 STMBench7

2 Performance results examples

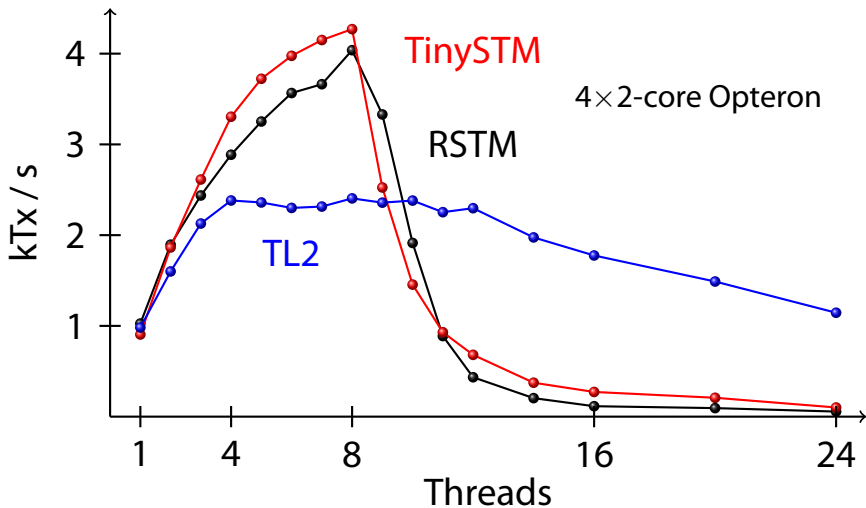
# Lock-Based vs. Obstruction-Free

Urban legend:

obstruction-free TMs inherently slow

lock-based TMs much faster

# Lock-Based vs. Obstruction-Free

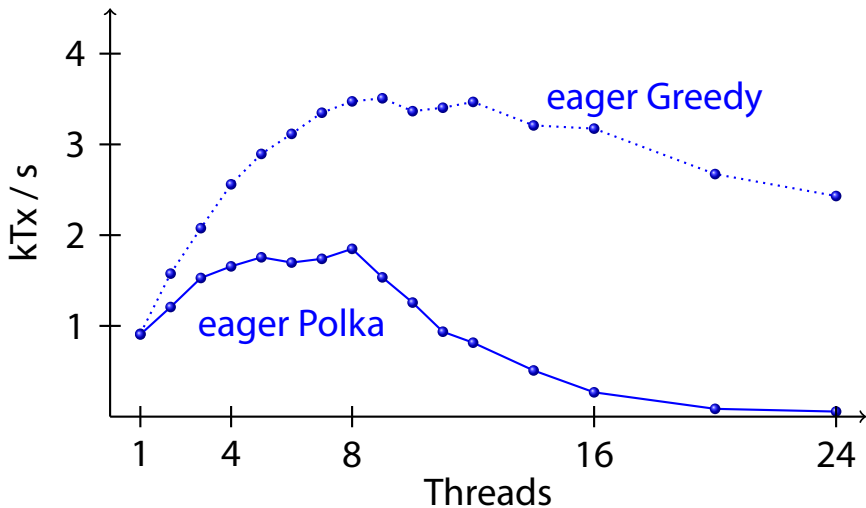


# Contention Management

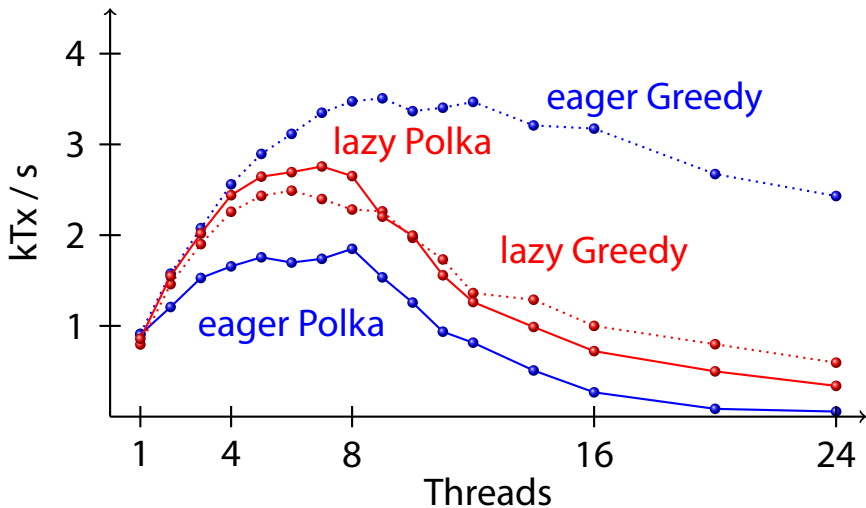
Contention management  
and  
Conflict detection mechanism

How are those connected?

# Contention Management



# Contention Management



# Performance: General Observation

Policy



Per-access overhead

# Summary

## STMBench7

a benchmark for all TMs

Evaluate performance & usability

in a (possibly) realistic setting

(and discover bugs...)

# STMBench7

`lpd.epfl.ch/site/research/tmeval`

free (BSD-style license)